

## REMARKS

Claims 54-65 have been added and claim 53 has been canceled. Claims 51, 52 and 54-65 remain in the application. Reconsideration of the application in view of the amendments and the remarks to follow is requested.

Claims 51-53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Koh et al., U.S. Patent No. 5,686,337, Chan et al., U.S. Patent No. 5,627,094, Rosner, U.S. Patent No. 5,496,757 or Kim, U.S. Patent No. 5,403,767.

Claim 51 recites "etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", which is not taught or disclosed by any of the cited references.

The Examiner's rejection based on Koh et al. demonstrates on its face that Koh et al. do not teach, disclose, suggest or motivate the invention as recited in claim 51. The Examiner indicates that the etching steps are shown in Figs. 3 and 5, while the insulative partitions are shown in Fig. 7, corresponding to a processing step subsequent to the etching steps.

Chan et al. teach formation of a patterned planarized first dielectric layer 20b in a first anisotropic etching step (Fig. 2b; col. 8, lines 25-35). This step also defines capacitor container openings. As a result, Chan et al. do not and cannot teach, disclose, suggest or motivate the invention as recited in claim 51.

The Examiner's rejection based on Rosner demonstrates on its face that Rosner does not teach, disclose, suggest or motivate the invention as recited in claim 51. The Examiner indicates that the etching steps are shown

in Figs. 4 and 5, while formation of the insulative partition is shown in Fig. 6, corresponding to a processing step subsequent to the etching steps. Rosner does not teach or disclose formation of an insulative partition intermediate two etching steps as recited in claim 51.

Kim '767 teaches etching first openings in an insulating layer 7 in Fig. 1C. The first openings are not capacitor container openings. Kim '767 then teaches formation of "second insulating film spacers 8A" followed by formation of "etching barrier layer 9" (Fig. 1D; col. 2, lines 42-57). Kim '767 teaches formation of capacitor containers in Fig. 1E by removal of the remainder of the insulating layer 7A, i.e., in a single etching step. As a result, Kim '767 does not and cannot teach, disclose, suggest or motivate formation of insulative partitions between two separate etching steps, as recited in claim 51.

For at least these reasons, the rejection of claim 51 is in error and should be withdrawn, and claim 51 should be allowed.

Dependent claim 52 is allowable as depending from an allowable base claim and for its own recited features which are neither shown nor suggested by the prior art.

New claims 54-65 are supported by text appearing at p. 6, line 2 through p. 18, line 9 of the application as originally filed. No new matter is added by new claims 54-65. New claims 54-65 distinguish over the art of record and are allowable.

Further, Applicant herewith submits a duplicate copy of the Supplemental Information Disclosure Statement and the Form PTO-1449 filed together in this application on January 25, 2001. No initialed copy of the

PTO-1449 has been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

In view of the foregoing, allowance of claims 51, 52 and 54-65 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

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By: 

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